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# SOC Implementation of Dynamic Reconfiguration of Approximate Arithmetic Units for MPEG Encoder

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**ABSTRACT:** This project mainly focuses on the realization of an efficient logic design of MPEG encoder with dynamic reconfigurable techniques. The fixed approximate hardware is used for an MPEG encoder increases the output qualities of the different input videos. The main reason for this output quality fluctuation is that the degree of approximation(DA) in the hardware architecture is fixed statically and cannot be customized for different inputs. It is simulated using NC (Native code complier) of cadence and synthesized using RC (RTL code complier) of cadence tool. The physical layout is designed for arrangement of standard cells (PD-physical design) in cadence. Although the proposed dynamic reconfigurable approximate architecture can easily extended to other DSP applications.

**KEYWORDS:** MPEG encoder, Motion estimation, DWT, IDWT, Quantization, Degree of approximation(DA), matlab-14b, verilog HDL, NC, RC, Physical design.

## I.INTRODUCTION

Images and videos are varies in a variety of properties, such as color, resolution, brightness, contrast, saturation, blur, format, and so on. A naive static approximation technique, which offers suitable viewing quality for some specific types of videos, will fail to give adequate quality for some others. Specifically, this paper makes the following contributions.

1) We demonstrate that, for a fixed level of hardware approximation in an MPEG encoder, the output quality varies widely across different videos, often going below acceptable limits. This shows that setting the level of hardware approximation statically is insufficient.

2) We suggest a design methodology to adapt the DA dynamically based on the video characteristics with the goal of confirming that output quality is within a definite bound.

## II. LITERATURE SURVEY

There has been a lot of effort in constructing energy-efficient video compression schemes. Many of them are linked to the specific case of an MPEG encoder. Different methods of power-reduction include algorithmic modifications , voltage over-scaling, and imprecise computation of metrics. An adaptive bit masking method is proposed , where the authors offer to truncate the pixels of the current and previous frames required for ME depending upon the quantization step. Video processing is a method used to analyze video streams electronically. It helps end-users to compress events which are unwanted in real time. Sequences of images, are actually called as videos, each of which called as a frame.

## HARDWARE IMPLEMENTATION

In this project for hardware implementation verilog code was written for the MPEG encoder block. The MPEG encoder architecture is implemented in cadence tool. Many software's consists in cadence tool. For this project tools

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were utilized was (NC- NATIVE CODE for Simulation), (RC- RTL complier for synthesis) and encounter digital implementation tool for soc (Physical layout of standard cells).

### LOGICAL IMPLEMENTATION

In this logical implementation the DWT is implemented in Matlab 14b by using simulink blocks. In similar way, logical implementation of IDWT is also implemented in matlab by using simulink blocks. Open Matalb 2014b in that open simulink where tool will be open in that click on DSP system tool box where we get simulink blocks.

## III. PROPOSED SYSTEM

### MPEG COMPRESSION SCHEME

MPEG has for long been the most preferred video compression scheme in modern video applications and devices.It has been proven that the ME and DWT blocks are the most computationally expensive components of an MPEG encoder. The different steps involved in performing MPEG compression are shown in fig 1.

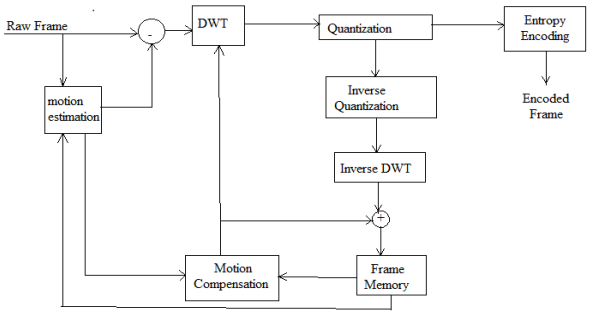


Fig .1 MPEG encoder block diagram

### RECONFIGURABLE ADDER/ SUBTRACTOR BLOCKS

This reconfigurable architecture can include any approximate version of the adders/subtractors. we have chosen the two most naive methods presented in [2], namely, truncation and approximation 5, for approximating the adder/subtractor blocks.

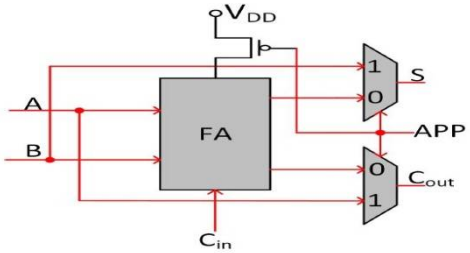


Fig . 2 1-bit DMFA

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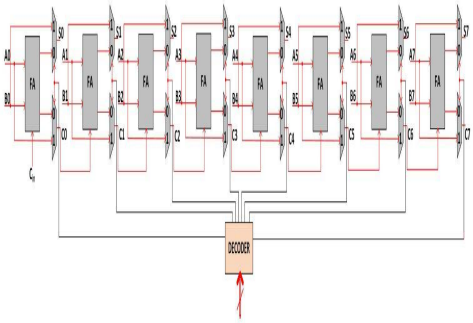


Fig .3 8-bit reconfigurable RCA block

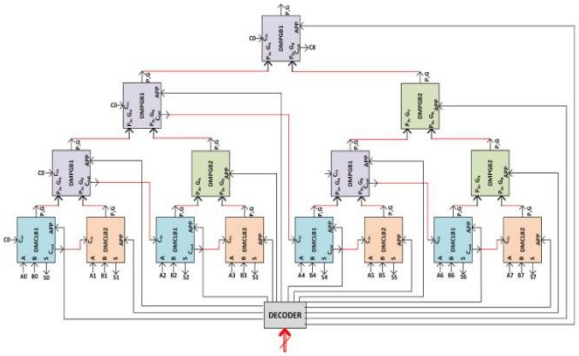


Fig. 4 8-bit reconfigurable CLA block

## MOTION ESTIMATION

### FULL-SEARCH BLOCK-MATCHING ALGORITHM

The motion estimation of MPEG-4 encoder accepts as inputs in macroblocks of the current frame and the pixels in the search area of the reference frame.

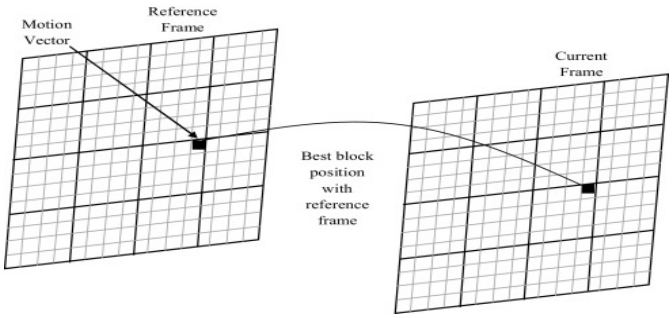


Fig .5 Process of motion estimation

Fig.5 shows that a macroblock and corresponding search area for N=3 and p=2. In that figure m(i,j) means each pixel in the macroblock, s(i,j) mean each pixel in the search area. The search area contain (N+2p)*(N+2p) pixels. Note that SAD (Sum of Absolute Difference) is generally used for the matching criterion and is given as

$$SAD(x,y) = \sum \left| m(i,j) - s(i+x, j+y) \right| \quad \text{for } -p \leq \{x,y\} \leq p$$

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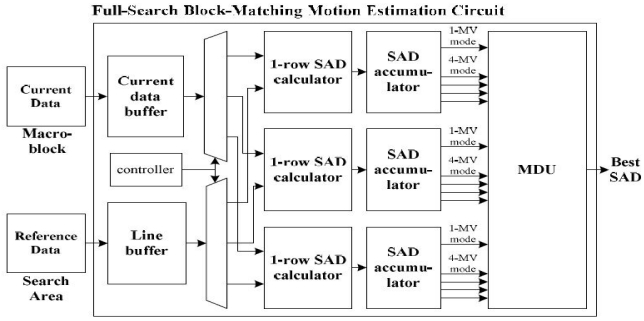


Fig.6 Proposed architecture of motion estimation circuit

## DISCRETE WAVELET TRANSFORM

The Discrete Wavelet Transform has become powerful tool in a wide range of applications including image/video processing [14], numerical analysis and telecommunication. The advantage of DWT over existing transforms, such as discrete Fourier transform (DFT) and DCT, is that the DWT performs a multi-resolution analysis of a signal with localization in both time and frequency domain.

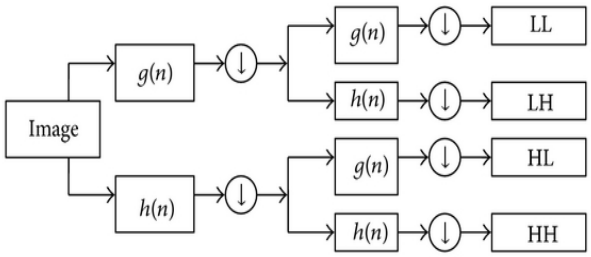


Fig.7 Discrete wavelet transform circuit

## QUANTIZATION

Quantization is the process of selectively discarding visual information without a significant loss in the visual effect. Quantization reduces the number of bits needed to store an integer value by reducing the precision of the integer.

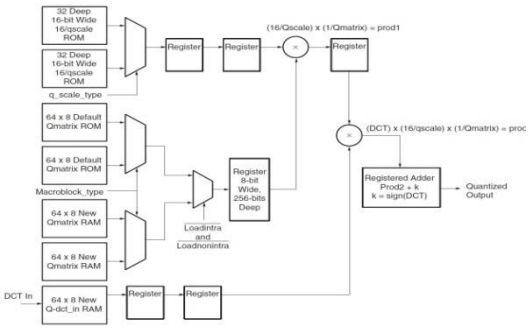


Fig.8 Implementation of Quantizer circuit

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**INVERSE QUANTIZATION**

A mismatch control is applied to the output of the inverse quantization.

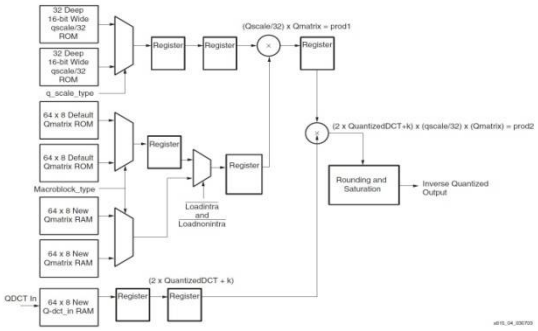


Fig.9 Implementation of inverse quantizer circuit

**INVERSE DWT**

Once we arrive at our discrete wavelet coefficients, we need a way to reconstruct them back into the original signal (or a modified original signal if we played around with the coefficients). In order to do this, we utilize the process known as the inverse discrete wavelet transform.

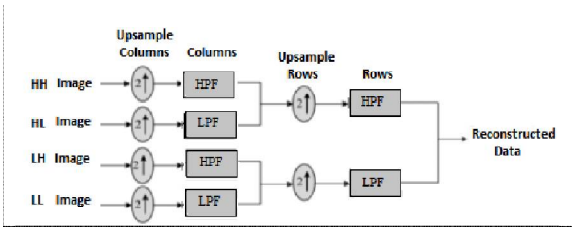


Fig.10 Inverse DWT circuit

## IV. EXTENTION

**DWT Implementation Using Matlab2015b Software**

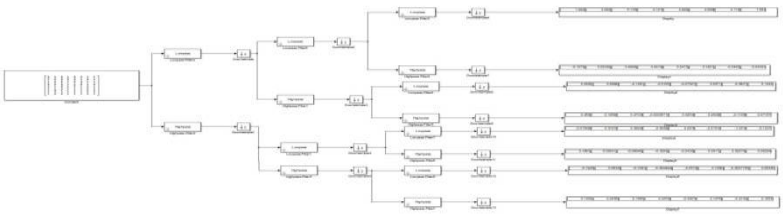

Fig.11 Implementation of DWT

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## IMPLEMENTATION OF INVERSE DWT USING MATLAB2015B SOFTWARE

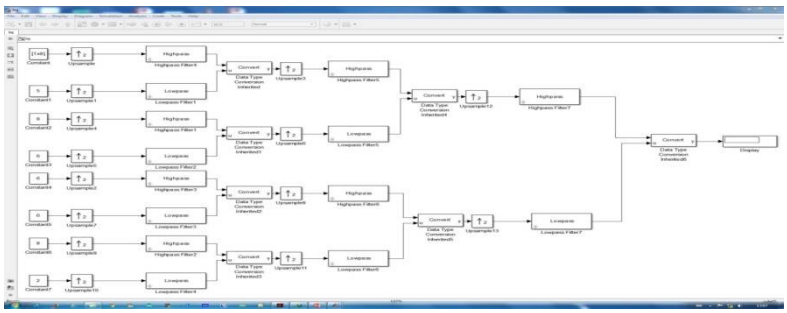

Fig.12 Implementation of inverse DWT

## APPLICATION

This project shows how to compress a video using motion compensation and transformation technique. It calculates motion vectors between successive frames and uses them to reduce redundant information.

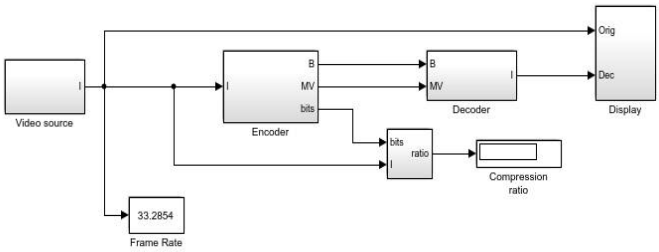


Fig.13 matlab simulink model for video compression

## RESULTS

### XILINX RESULTS: SIMULATION RESULT

The Xilinx outputs for the proposed system are shown in below figures.

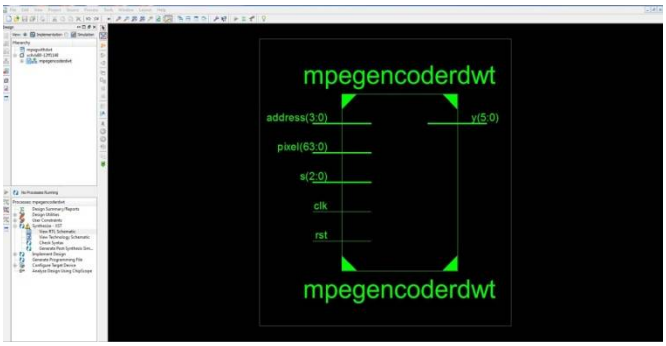


Fig.14 RTL schematic for MPEG encoder

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## NATIVE CODE RESULTS (CADENCE): SIMULATION RESULT

In the native code the simulation results will be shown. The figure 6.4 shows the MPEG encoder simulation results.

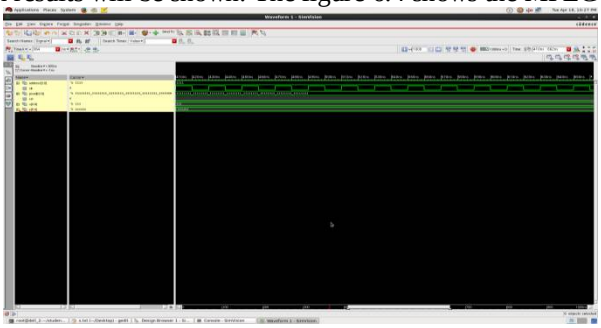

Fig.15 simulation results using cadence tool

## RC (RTL) SCHEMATIC FOR MPEG ENCODER

After finishing the Native code simulation, we have to check the schematic. So for that we should use the RTL compiler.

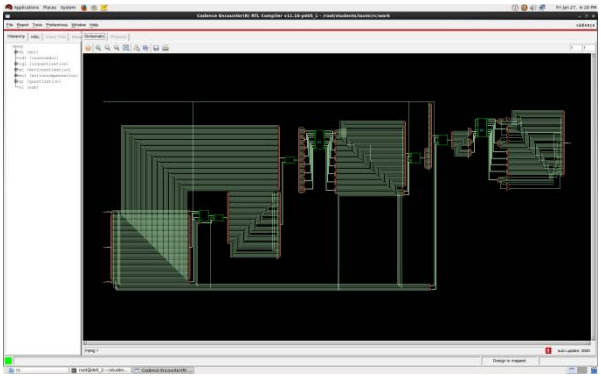

Fig.16 RTL schematic for MPEG encoder using RC tool

## PHYSICAL DESIGN FOR SYSTEM ON CHIP

**SoC Encounter** for backend design (floorplanning, place and route, power and clock distribution.

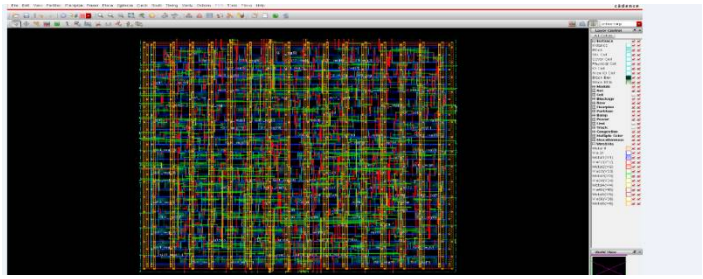

Fig.17 Gates placed with clock tree

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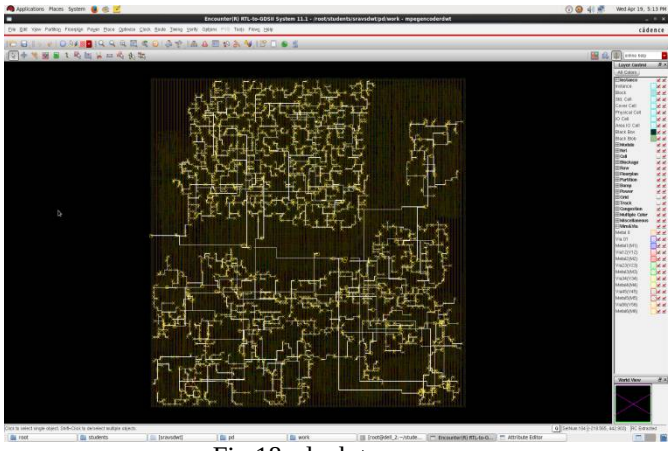

Fig.18 clock tree

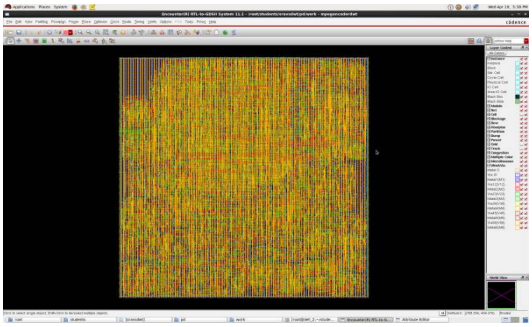

Fig.19 SOC final CHIP

**POWER AND AREA RESULTS**

Power Analysis:

| S no | Technology | Leakage power | Dynamic power | Total power |
|---|---|---|---|---|
| 1 | 180nm | 1741.504 | 65072219.241 | 65073960.745 |

Area Analysis:

| S no | Technology | Area |
|---|---|---|
| 1 | 180nm | 322395 |

## V. CONCLUSION

In this paper proposed Dynamic reconfigurable approximate architecture for the MPEG encoder that optimizes the power consumption while maintaining the quality across the different videos. Our experiments shows that the proposed reconfigurable architecture results in power savings while maintaining the quality. By using the DWT

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transformations, the encoder provides the quality in its output. The system on chip (SoC) **180nm** uses the constant voltage scaling technique to provide a low power implementation. The system on chip (SoC) 180nm provides to reduce the power consumption, area and timing analysis.

## VI. FUTURE WORK

Future work includes the incorporation of other approximations and extending the approximations to the other arithmetic and functional blocks. Although the Dynamic reconfigurable approximate architecture can easily extended to the other DSP applications.

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## BIOGRAPHY

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**Dr.B.K. Madhavi** ,a recipient of Ph.D Degree from JNTUH, Hyderabad in the area of" Low Power VLSI Design" during the year 2007. She published around 85 papers in the national and international journals & conferences. She is guiding 12 Ph.D scholars in the area of VLSI & Nanotechnology and two Scholars were already awarded Ph.D from JNTUH. Presently she is working as professor in the department of ECE in the Sridevi Women's Engineering College, Hyderabad.